

A Design Framework for Carbon Nanotube Circuits Affixed on DNA Origami Tiles: Extended Abstract

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Recent years have witnessed a burst of experimental activity concerning algorithmic self-assembly of nanostructures, motivated at least in part by the potential of this approach as a radically new manufacturing technology. Our specific interest is in the self-assembly of Carbon-Nanotube Field Effect Transistor (CNFET) circuits. One of the presently most reliable self-assembling, programmable nanostructure architectures is DNA origami [7]. Several authors have announced the formation of DNA origami tiles, capable of further assembly into larger, fully addressable, 1D and 2D scaffolds [2, 4, 6]. Such scaffolds make possible the construction of highly complex structures on top of them [5], prospectively including nanocircuits.

CNFET circuits have been previously introduced on top of addressable DNA lattices [1]. While such large lattices ($2\text{--}5\ \mu\text{m}$) are experimentally achievable, the uniformity of their structure as well as the fact that the entire circuit must assemble simultaneously, makes the functionalisation of the lattice difficult. In the present work, we propose a generic framework for the design of CNFET circuits comprising a “universal” set of 14 functionalised DNA origami tiles shown in Figure 1. The marks on the tiles indicate the arrangements of the CN’s affixed on the respective DNA origami; with a proper selection of “glues” on the tiles, any desired CNFET circuit can be self-assembled from this basis.

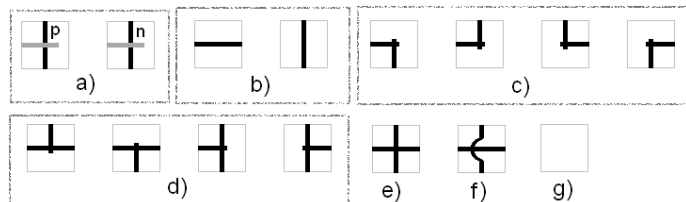


Figure 1: The 14 tile types and the blank tile, out of which any CNFET circuit can be assembled.

One advantage of this approach is that it decouples the self-assembly aspects of the manufacturing process from the transistor circuit design. It also supports efficient high-level analysis of the purported circuits, both by computer simulations and by analytical means. For instance, all assembly errors can at this level be treated as tiling errors, leading to a transparent design discipline for fault-tolerant architectures.

We now briefly outline some of the details of our approach and give a few examples. The tile types indicated in Figure 1 are: a) p-type and n-type CNFETs, b) straight (horizontal or vertical) CN wires (CNWs), c) corner CNWs, d)-e) 3- and 4-way junction CNWs, and f) crossing but non-interacting CNWs. Additionally, when analyzing fault tolerant architectures, it is convenient to introduce also a blank tile (Figure 1 g). In order to design a particular nanocircuit, one first prepares the transistor circuit design using the 14 basis tiles indicated. Then, an optimal number of glues for these tiles is computed and finally, appropriate sticky ends are designed for the DNA origami tiles. In this abstract, we concentrate on the circuit design aspect; for selecting an optimal number of glues, see e.g. [3]. In Figure 2 we present the designs for a CMOS inverter and NAND gate. The inverter constitutes a $3 \times 2 = 6$ tile

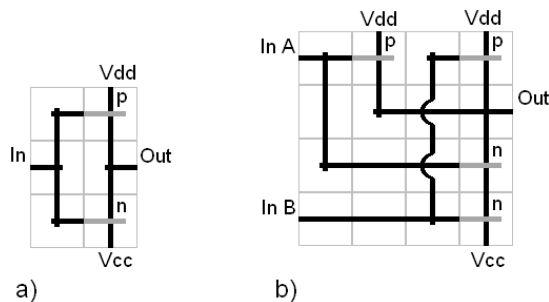


Figure 2: a) The design out of DNA origami tiles of a) a CMOS inverter, and b) a CMOS NAND gate.

assembly and the NAND gate correspondingly a $4 \times 4 = 16$ tile assembly.

To illustrate how our approach supports the design of fault-tolerant circuit architectures, let us assume that the CN acting as gate in a CNFET does not attach to the DNA origami. Then this tile will act as a vertical CNW tile. Similarly, if one metal nanoparticle is not attached to a 3-way junction CNW tile, depending on its position, we will obtain either a corner CNW tile, or a straight CNW tile. In the worst case, if the functionalisation of a tile is highly altered, the tile can be considered blank. Based on the Quadded Transistor (QT) model [8], we have prepared several fault tolerant circuit designs and analyzed their reliability. For instance, Figure 3 presents tiling designs for a QT transistor structure and a fault-tolerant CNFET CMOS inverter based on this. In both designs, if any one tile is replaced, the output of the entire device is still preserved. In a similar way, fault-tolerant designs for more complicated devices such as CMOS NAND and NOR gates can be achieved, and their error probabilities estimated. We have also introduced a general algorithm for approximating the actual error probability of any CNFET circuit assembled in our framework.

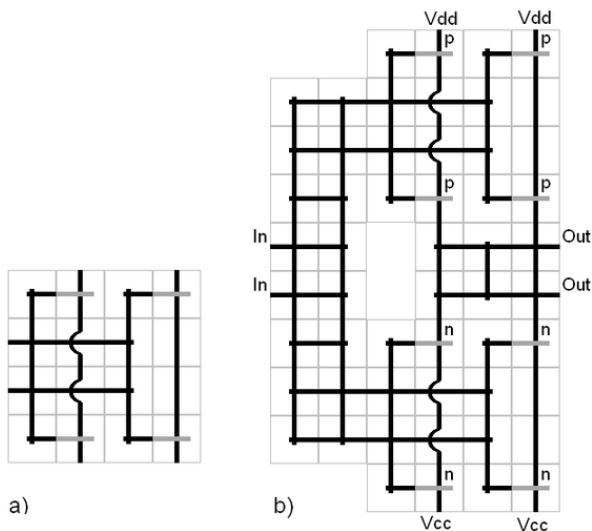


Figure 3: a) Implementation of the QT structure. b) A fault tolerant inverter; even if several tiles have errors, the gate is still giving the correct output.

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